ASIC Designers Voyage Beyond IC's Edge

by Lisa Schaerti and Hemant Shah

In ages past, explorers drew maps constrained by their own knowledge and experience. At the edges of the known world began a vast undefined space, marked with the warning: "Here be dragons."

For today's IC and ASIC designers, the edge of the IC might as well be the end of the known world. What happens to a signal when it heads into the uncharted territories of the IC package, the printed circuit board, and the world beyond? Will it reach its destination safely, and on time?

The answer matters far more than most IC designers realize. Although they may not be afraid of the dragons in the printed circuit board, they are generally more than happy to let someone else deal with them. This approach has worked so far. But to chart new territory in electronic design, we have to expand the horizon. Like the explorers of old, we'll have to face the dragons.

It's Just Boards— How Hard Can That Be?

The IC design community holds a belief that chip design is the truly hard part of electronic system design. Cranking out a printed circuit board design is dismissed as a relatively simple job: just place all the components after the chip is finished. In reality, what happens on the board will make or break your IC in the real-world system, and you had better account for its impact early on. It's shortsighted to finish the IC design and then leave it to others to:

- Make it fit in the targeted phone, laptop, and so forth
- Ensure that its performance is not reduced by board effects
- Keep the system costs within the targeted range
- Get it to market by Christmas

If your company's end product is a system, your success depends on the entire system—not just the IC—successfully passing the above four tests of form factor, performance, cost and time to market. And if you're a pure chip vendor, helping your systems customer meet these challenges gives you a major competitive advantage over those who supply chips as a commodity.

Mapping the Territory

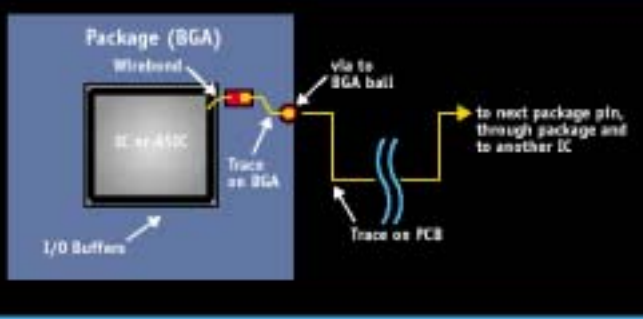
Let's begin by charting the territory *(Figure 1)*. The IC is at the center of the universe, with the die pads placed at the convenience of the IC designer. Through state-of-the-synthesis, place and route, and simulation tools, we're confident that we have beautiful GHz signals across the chip.

What's next? A package is needed to protect the IC from the elements and bring its signals to a more robust connector. For high-pin count devices with thousands of I/Os, a ball grid array (BGA) package is the natural choice.

The printed circuit board next comes into play. The signal must travel across the board with minimal distortion to

Figure 1

Mapping the Territory

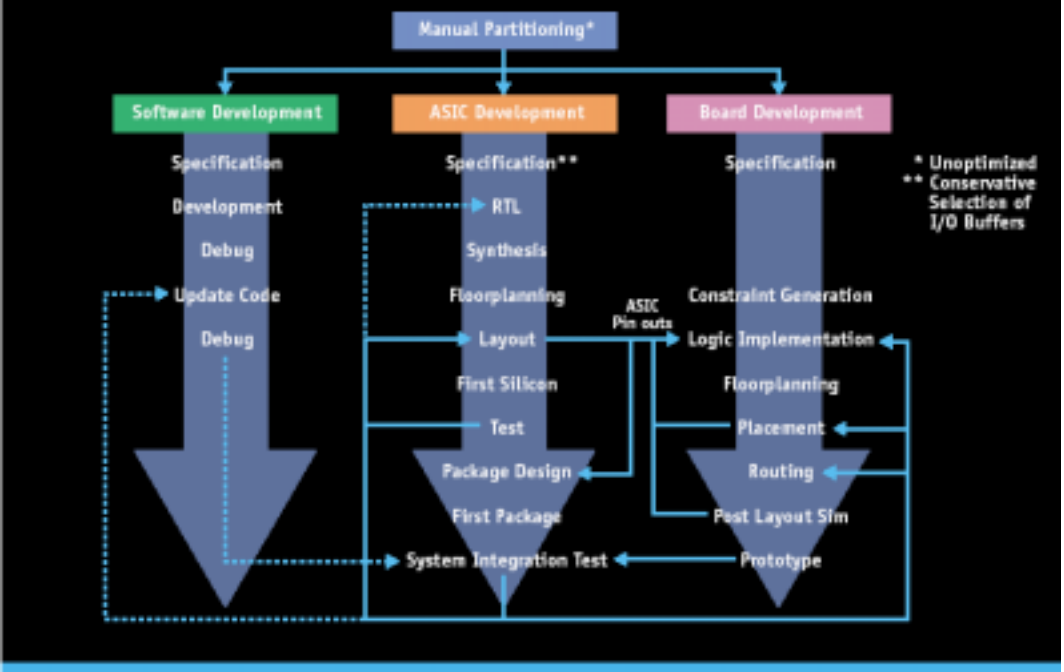


Critical signals cross several physical boundaries from the edge of the IC to their final destination. Board and connector effects, different material dielectrics, EMI and signal integrity all impact the IC performance in real-world systems. IC and ASIC designers would do well to consider these effects.

reach another IC or the outside world. How do we ensure that ground bounce, reflections, electromagnetic interference and simultaneous switching noise on the board do not cause unacceptable performance degradation?

Figure 2

Traditional Design Flow



Traditional IC, package and board design are separate processes with many iterations built into each. The results are sub-optimal IC pin outs, longer board design cycles, and board designs that eat into the performance that the IC design team worked so hard to achieve.

Today the IC and board are developed by separate design teams, tool sets and flows (*Figure 2*). Very little data is exchanged until the final step—system integration and test.

In a new approach, IC and board design teams share information in the planning stages, making trade-offs that cross the IC-board boundary to optimize performance, size, and cost of the system *(Figure 3*).

Charting New Course

Thomson Consumer Electronics has taken this new course in its latest products for the HDTV market. Thomson engineers develop specifications for ASICs that will be built by vendors and integrated into Thomson end products. Using the traditional process, the engineer would have no data as to what load the ASIC I/O would drive. Therefore the safe course is to specify I/O buffers with the highest drive.

Unfortunately this creates really big “dragons” for engineers in the board design space in terms of electromagnetic interference (EMI) and signal integrity (SI) problems. The design takes longer because of its complexity, and performance is harder to ensure. Maximum-strength drivers usually require terminators on the board to manage signal integrity. Those few components take up valuable real estate and translate to extra costs per unit that are nontrivial in a highly competitive consumer electronics marketplace.

Optimized Buffer Strength

On a recent ASIC project, Thomson engineers used Avant!’s EDA*navigator* to specify the needed buffer strength. EDA*navigator* is an engineer’s tool for design planning and early analysis of printed circuit boards. It is key to developing an ASIC board co-design methodology.

To get started, the engineer reads a schematic with the ASIC symbol and the loads it will drive. Because the ASIC is not yet designed, no physical footprint is available. The engineer uses EDA*navigator* to synthesize a shape, place the critical components on the board, and determine the net topology to meet

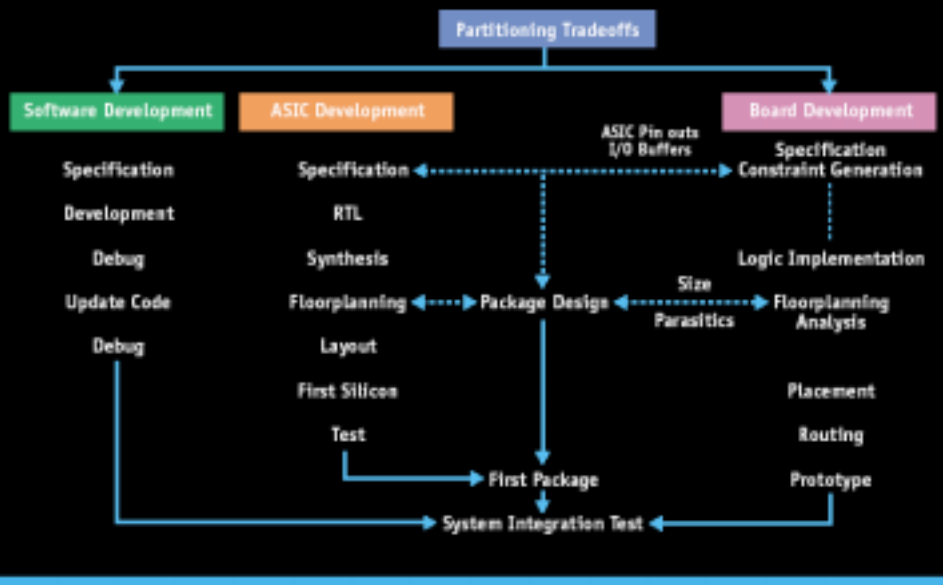
the other design constraints for critical nets. EDA*navigator's* first-order advisors provide real-time feedback during critical component placement and modification.

Once the placement is within tolerance for delay and skew, engineers use analysis tools integrated with EDA*navigator* to identify any problems with reflections.

The ideal solution is to choose enough drive strength in the I/O buffer for all applications without requiring any terminators. To determine whether this ideal can be achieved, engineers can manipulate critical component placement to minimize net lengths, explore alternate net topologies, or choose different IBIS models to characterize the available I/O buffers.

Figure 3

IC-Board Codesign Flow



New IC package and board co-design approach allows system designers to avoid unnecessary iterations, optimize pin-outs, and ensure that the critical signals reach their destination without unnecessary performance losses.

EDA*navigator* provides all of these options in an intuitive environment on the engineer's desktop. With easy access to third party analysis tools, the engineer can make changes within EDA*navigator* and very quickly get feedback on reflections and other factors.

In this case the ideal trade-off solution was achieved, avoiding unnecessary terminators on the board. These few hours of up-front analysis with EDA*navigator* helped reduce the cost of the end product without impacting the cost or development schedule of the ASIC. This translates into increased profit margins and/or a lower price point for the product in a hyper competitive market.

Optimizing Pinouts

Next, the Thomson engineer uses EDA*navigator* to specify the optimum ASIC pin outs. With critical components placed on the board, EDA*navigator* determines an ASIC pin-out configuration that allows for optimized routing on the board.

This process takes a few minutes, and for complex boards can save days to weeks of routing iterations. Pin-out specification can be passed on to the ASIC vendor.

Sailing Toward Tomorrow

This IC-package-board concurrency avoids surprises late in the product development cycle, when the IC and board finally come together for final integration and test.

For IC designers, the concurrent design process offers a unique opportunity to ensure that the signal reaches its destination without unacceptable distortions or delays.

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