Building a Smarter Cockpit

A team of avionic systems engineers at Honeywell have used design automation software to revolutionize the way pilots fly planes.

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Honeywell Business and Commuter Aviation Systems (BCAS) engineers face the need to pack more performance into smaller products, with higher speeds and lower costs. In this regard they're not much different from their colleagues in the wireless, consumer and other high-end electronics markets. What's noteworthy is the way they've applied new design automation software to improve their design process and results.

Their latest product, the Primus Epic avionics suite, "promises nothing short of a revolutionary change in the way pilots manage cockpit information," says Thomas Horne of *AOPA Pilot*. The system displays movable navigation maps, ground-based weather, real-time video and aircraft utility system information on up to six large (8x10-inch) flat panel LCDs. Pilots control many of the aircraft functions using touch pad displays, joysticks or trackballs in addition to traditional controllers.

The performance improvements over previous generation systems are impressive. An aircraft-wide network eliminates many dedicated point-to-point wiring requirements and significantly reduces wire weight, power use and installation costs. In addition, a unique modular framework makes the Primus Epic suitable for anything from light turboprop regional aircraft to heavy-class business jets.

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From the outset of this project, BCAS engineers were challenged with higher clock speeds, reducing system size and weight by 40%, reducing costs 30 to 50%, and improving reliability and maintainability over previous systems. These goals meant they needed to approach the design process differently if they were to meet their delivery schedules. A major part of this change was introducing Xynetix's EDA*navigator* software for design planning and early analysis of their printed circuit boards.

"EDA*navigator* allows us to design more robust products in less time," says Bob Quirk, principal engineer at Honeywell BCAS. "The way it improves our design process has been key to meeting the Primus Epic design goals."

Analysis made less painful

With clock speeds increasing with each new design, physical effects have significant impact on system performance, Quirk explained. Engineers can't easily predict what these physical effects will be until after they've turned over their logic design to the CAD group and the board layout is substantially finished. Then they can use various analysis tools to look at timing, signal integrity, crosstalk, thermal dissipation, routability, and other issues. They usually build several prototype boards for lab testing, as well.

There are several problems with this approach. One, it forces engineers to look at each constraint in isolation of other, often conflicting constraints. This means they may solve a timing problem only to discover (much later) that they've created a routing problem. Two, the analysis comes late in the design process, when changing the board causes significant delays and expense. Parts may already be on order, changes are expensive and painful, and engineers end up making less-than-optimal work-arounds that can increase manufacturing costs or compromise performance. Finally, the various analysis tools can be difficult for non-specialists to use, and the physical prototypes are expensive.

EDA*navigator* addresses these problems by making analysis software easier to use, and integrating them into the early design planning stages, when it's easier to explore options and make changes. Perhaps more importantly, it lets engineers run analysis on several constraints simultaneously in order to make design trade-offs. For example, they can evaluate how different partitioning strategies affect cost (e.g. number of layers) and performance before sending the design to the layout group. This eliminates iterations and shortens time to production.

"We begin our designs by using EDA*navigator*'s Net Explorer," Quirk said. Net Explorer includes a net topology editor, an electronic constraint manager and various analysis engines to let engineers explore net topologies and define high speed constraints before the schematic is completed or packaged.

"Being able to make net- and part- changes in our schematic capture environment and having these changes immediately accessible in EDA*navigator* is a great help," Quirk said. "It saves time and allows us to easily study what-if scenarios."

Applying the tools

Next BCAS engineers use EDA*navigator* to do density studies. This simple step takes only a few hours of the engineer's time, yet helps avoid days of iterations between engineering and layout. If a problem with density is predicted, engineers can explore options such as changing part selections, adding layers or implementing a multi chip package or daughter card. They can evaluate the cost and performance implications of these trade-offs before sending the design on to the circuit card design group. "It's nice to know all the parts will fit before beginning the formal design," Quirk said.

Using EDA*navigator* in this way helps maximize density, which was a key to achieving the goal of 40% reduction in system size. "We knew up front the board usage, and in some cases were able to add functionality based on the knowledge of having additional room to work with," Quirk said.

Next BCAS engineers use EDA*navigator* to do preliminary placement and define critical layout constraints. The engineer defines a known partition (e.g., the analog section), draws a room outline near a fixed connector, and indicates which key components must go into this partition. EDA*navigator* can automatically group the remaining components into partitions based on their interconnect and other constraints, or the engineer or layout designer can do this step interactively. "This allowed us to have more logical partitioning, which also reduced overall complexity and cost," Quirk explained.

During net topology exploration, area studies and partitioning, engineers capture critical constraints using EDA*navigator's* Constraint Manager, a spreadsheet-based electronic file that is later passed electronically to the layout group. Combined with EDA*navigator's* analysis tools, it lets engineers define the constraints so as to provide as much margin for the PCB designer as possible, while ensuring that electrical performance meets design goals.

"Handling high resolution, true color digital video in real time required us to use bus bandwidths as high as 100Mbytes/second," Quirk said. "We were able to constrain these buses to ensure that things like skew and impedance were properly controlled, without over-constraining the design for the layout designers.

The Constraint Manager can also incorporate manufacturing rules and many other constraints. Default values allow engineers to begin using it immediately. With its hierarchical structure, each constraint can be applied to the entire design or modified for an individual partition, netclass, net or pin pair. This saves time and improves accuracy by reducing the number of rules to be managed.

Passing EDA*navigator* data, including critical placement data and the constraints file, to the design group electronically has several benefits. "Communication between the engineers and the circuit card designers became clearer," said Quirk. "We have much higher confidence that our constraints are workable, and we are able to prevent the errors and iterations that we used to get when we shared constraint information verbally."

Finally, EDA*navigator* allows for quick but detailed board checking after layout. Engineers can bring up the layout file from within EDA*navigator* and easily view all nets that have signal integrity constraints. Rules and actuals for each net can be displayed side-by-side, so engineers can quickly see whether the original criteria were met.

Changing design environment

Using EDA*navigator* has helped Honeywell BCAS improve design performance, density and costs while shortening design time. It also facilitates design reuse, since the placement information and constraints can be reused during an ECO cycle or a revision of the design months later. "We were able to assure consistent performance on reused circuitry by using the same placement and routing from a baseline design," Quirk said.

Changing the design process at Honeywell BCAS involved integrating new software into the existing design environment, educating engineers on its benefits, and convincing design teams to change established routines. The results have been well worth the effort. Said Quirk, "Most all of our new products will be developed with the aid of EDA*navigator*."

References: "Honeywell's Primus Epic CDS Brings Tomorrows Functionality into Today's Cockpits," www.cas.honeywell.com/bcas/news, Sept. 1997

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